APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,778	05/03/2001	Peter A. Beerel	06666-077001/USC3027	6633

20985 7590 04/19/2005	EXAMINER
FISH & RICHARDSON, PC	TORRES, JOSEPH D

12390 EL CAMINO REAL	ART UNIT	PAPER NUMBER
SAN DIEGO, CA 92130-2081	2133	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>21 March 2005</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>*1-19 and 36-102*</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>*1-19 and 36-102*</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>06 July 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>03/21/2005</u>.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

Response to Arguments

1.   Regarding arguments concerning 112 issues:

The Applicant contends, "As per the remaining rejections, the Examiner confirmed that

amending the application to include 'a tree structure arranged to perform parallel prefix

and suffix operations' should be sufficient to overcome the rejections regarding the use

of the term 'a tree structure arranged in a parallel prefix and suffix architecture' and

similar claim language".

The Examiner would like to point out that it was the Examiner's understanding that the

language, starting at line 18 on page 21, defining suffix operations, "Similarly, a suffix

operation can be defined as a generic form of computation that takes in n inputs...", that

the language would be amended to explicitly define suffix operations, that is, it was the

Examiners understanding that the language would be modified to read --Similarly, a

suffix operation ~~can be~~is defined as a generic form of computation that takes in n

inputs...--.

The examiner does agree with such amended language the definition of suffix operation

is no longer indefinite.

Applicant's arguments with respect to claims 1-19 and 36-102 have been considered

but are moot in view of the new ground(s) of rejection.

Specification

2.   The Applicant contends, "As per the remaining rejections, the Examiner

confirmed that amending the application to include 'a tree structure arranged to perform

parallel prefix and suffix operations' should be sufficient to overcome the rejections

regarding the use of the term 'a tree structure arranged in a parallel prefix and suffix

architecture' and similar claim language".

The Examiner would like to point out that it was the Examiner's understanding that the

language, starting at line 18 on page 21, defining suffix operations, "Similarly, a suffix

operation can be defined as a generic form of computation that takes in n inputs...", that

the language would be amended to explicitly define suffix operations, that is, it was the

Examiners understanding that the language would be modified to read --Similarly, a

suffix operation ~~can be~~is defined as a generic form of computation that takes in n

inputs...--.

The examiner does agree with such amended language the definition of suffix operation

would no longer be indefinite and would comply with the enablement requirement of 35

U.S.C. 112, first paragraph. When the **written record** clearly provides an unambiguous

definition of "suffix operation", the Examiner will withdraw all objections to the

specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of
making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
set forth the best mode contemplated by the inventor of carrying out his invention.

3.   Claims 1-19, 36-90, 92, 94, 96, 98, 100 and 102 are rejected under 35 U.S.C.

112, first paragraph, as failing to comply with the enablement requirement. The claim(s)

contains subject matter which was not described in the specification in such a way as to

enable one skilled in the art to which it pertains, or with which it is most nearly

connected, to make and/or use the invention.

The Applicant contends, "As per the remaining rejections, the Examiner confirmed that

amending the application to include 'a tree structure arranged to perform parallel prefix

and suffix operations' should be sufficient to overcome the rejections regarding the use

of the term 'a tree structure arranged in a parallel prefix and suffix architecture' and

similar claim language".

The Examiner would like to point out that it was the Examiner's understanding that the

language, starting at line 18 on page 21, defining suffix operations, "Similarly, a suffix

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the language would be amended to explicitly define suffix operations, that is, it was the

Examiners understanding that the language would be modified to read --Similarly, a

suffix operation ~~can be~~is defined as a generic form of computation that takes in n

inputs...--.

The examiner does agree with such amended language the definition of suffix operation

would no longer be indefinite and would comply with the enablement requirement of 35

U.S.C. 112, first paragraph. When the **written record** clearly provides an unambiguous

definition of "suffix operation", the Examiner will withdraw all 35 U.S.C. 112, first

paragraph rejections of the claims.

Since the Applicant has made clear the Applicant's intention in the Interview on

03/04/2005, the examiner will proceed with the intended definition as stated, above.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.   Claims 1-19, 36-90, 92, 94, 96, 98, 100 and 102 are rejected under 35

U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and

distinctly claim the subject matter which applicant regards as the invention.

The Applicant contends, "As per the remaining rejections, the Examiner confirmed that

amending the application to include 'a tree structure arranged to perform parallel prefix

and suffix operations' should be sufficient to overcome the rejections regarding the use

of the term 'a tree structure arranged in a parallel prefix and suffix architecture' and

similar claim language".

The Examiner would like to point out that it was the Examiner's understanding that the

language, starting at line 18 on page 21, defining suffix operations, "Similarly, a suffix

operation can be defined as a generic form of computation that takes in n inputs...", that

the language would be amended to explicitly define suffix operations, that is, it was the

Examiners understanding that the language would be modified to read --Similarly, a

suffix operation can be is defined as a generic form of computation that takes in n

inputs...--.

The examiner does agree with such amended language the definition of suffix operation

would no longer be indefinite and would comply with the enablement requirement of 35

U.S.C. 112, first paragraph. When the **written record** clearly provides an unambiguous

definition of "suffix operation", the Examiner will withdraw all 35 U.S.C. 112, second

paragraph rejections of the claims.

Since the Applicant has made clear the Applicant's intention in the Interview on

03/04/2005, the examiner will proceed with the intended definition as stated, above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5.   Claims 1, 2, 6-12, 15-17, 19, 36-38, 42-47, 50-52, 61-63, 67-71, 74-76, 85-90,

93, 94, 97, 98, 101 and 102 are rejected under 35 U.S.C. 102(e) as being anticiapted by

Viterbi; Andrew J. et al. (US 5933462 A, hereafter referred to as Viterbi).

35 U.S.C. 102(e) rejection of claims 1, 8, 9, 12, 16, 17, 36, 37, 44-47, 51, 52, 61-62, 69-

71, 75, 76, 85-90, 93, 94, 97, 98, 101 and 102.

Viterbi teaches demodulating the received encoded signal to produce soft information

(See Figure 1 and 3 in Viterbi); and iteratively processing the soft information with one

or more soft-in/soft-output SISO modules (Figure 4 in Viterbi is a decoder having a

feedback loop for iteratively processing soft information according to the iterative

algorithm of Figure 7 in Viterbi; col. 3, lines 66-67 and col. 4, lines 66-67 in Viterbi teach

clearly suggest the intent to replace to replace the MAP decoders typically used in a

turbo decoder with SOVA decoders; Note: a SOVA decoder is inherently a decoder

accepting soft inputs to perform Viterbi's algorithm to produce soft outputs; hence a

SOVA decoder **is also a SISO decoder**; the Examiner suggests the Hagenauer treatise

included in the Examiner's PTO-892 for teachings on SOVA decoders), at least one

SISO module using a tree structure arranged to perform parallel prefix and suffix

operations to compute forward and backward state metrics (the Forward Viterbi

Decoder 24 in Figure 4 of Viterbi teaches a first SISO module using the Trellis tree

structure of Figure 5 to perform parallel prefix operations to compute forward state

metrics $\alpha_k(s)$ in Equation 5 in col. 6 of Viterbi and the Backward Viterbi Decoder 24 in

Figure 4 of Viterbi teaches a second SISO module using the Trellis tree structure of

Figure 5 to perform parallel suffix operations to compute backward state metrics $\beta_{k-1}(s')$

in Equation 6 in col. 6 of Viterbi; Note: the Applicant defines prefix operations

recursively as $z_0 = y_0$ and $z_i = y_0 \otimes \ldots \otimes y_i$, it is easy to see that Equation 5 in col. 6 of

Viterbi is a prefix operation by letting $z_0 = y_0 = \alpha_0$, k=i and $z_i = \alpha_i(s)y_i(s',s)$ when $\otimes$ is

multiplication, likewise equation 6 of Viterbi satisfies suffix operations if the suffix

operations are defined as on page 21 of the Applicant's disclosure).

In addition Viterbi teaches receiving an input signal corresponding to one or more outputs of a finite state machine (A convolutional encoder is inherently an FSM hence the received input signal corresponds to one or more outputs of a finite state machine: Note: a Trellis is also an FSM for the convolutional code).

Viterbi teaches receiving an input signal corresponding to output from one or more block encoding modules (col. 7, lines 40-44 in Viterbi teach one or more block encoding modules; Note: turbo encoders and SCIC codes are comprised of one or more block encoding modules).

35 U.S.C. 102(e) rejection of claims 2, 6, 7, 19, 38, 42, 43, 63, 67 and 68.

Page 6, line 5 of the Applicant's specification marginalization-combining operations-as is any pair of operations that satisfy the commutative semi-ring properties. Multiplication and addition over field elements used in the calculation of forward state metrics $\alpha_k(s)$ in Equation 5 in col. 6 of Viterbi backward state metrics $\beta_{k-1}(s')$ in Equation 6 in col. 6 of Viterbi are marginalization-combining operations since the Multiplication and addition are over a field and any field is a semi-ring.

35 U.S.C. 102(e) rejection of claims 10.

Note: claim 10 is an intended use claim. The Examiner asserts that the decoding devices in Viterbi are communication devices; hence using the decoding devices taught in Viterbi is an obvious embodiment of the teachings in Viterbi since that is what the

decoder is designed for and do not require any structural changes in the decoder taught

in the Viterbi patent. See Ex parte Masham, 2 USPQ2d 1647 (1987).

35 U.S.C. 102(e) rejection of claims 11.

See blocks 74 and 78 in Figure 7 of Viterbi.

35 U.S.C. 102(e) rejection of claims 15, 50, 59 and 74.

Note: a Brent-Kung tree is a specific obvious embodiment of a Trellis tree structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6.   Claims 3-5, 13, 14, 18, 39-41, 48, 49, 53-60, 64-66, 72, 73, 77-84, 91, 92, 95, 96,

99 and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viterbi;

Andrew J. et al. (US 5933462 A, hereafter referred to as Viterbi) in view of Benedetto et

al. (S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, Soft-Output Decoding

Algorithms in Iterative Decoding of Turbo Codes, TDA progress Report 42-124, Feb. 15,

1996).

35 U.S.C. 103(a) rejection of claims 3, 4, 39, 40, 64 and 65.

Viterbi, substantially teaches the claimed invention described in claims 1, 2, 6-12, 15-

17, 19, 36-38, 42-47, 50-52, 61-63, 67-71, 74-76, 85-90, 93, 94, 97, 98, 101 and 102

(as rejected above).

However Viterbi, does not explicitly teach the specific use of Min-sum operations.

Pages 72-73 of Benedetto, in an analogous art, teach max-sum operations. The

Examiner asserts that since $1/x$ is a minimum if x is a maximum so that use of min-sum

operations is an obvious embodiment of the teachings in Benedetto, since the

operations are inherently equivalent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify the teachings Viterbi with those of Benedetto by

including use of Min-sum operations. This modification would have been obvious to one

of ordinary skill in the art, at the time the invention was made, because one of ordinary

skill in the art would have recognized that use of Min-sum operations would have

provided the opportunity to to reduce the complexity for computing forward and

backward metrics since multiplication and addition operations are exchanged for

maximum and addition operations (see top of page 73 in Benedetto).

35 U.S.C. 103(a) rejection of claims 5, 41 and 66.

See equation 21 on page 72 of Benedetto.

35 U.S.C. 103(a) rejection of claims 13, 48 and 72.

Figure 6 on page 79 of Benedetto teaches using soft output of a first SISO as soft input

to another SISO.

35 U.S.C. 103(a) rejection of claims 14, 49 and 73.

The max-sum operations at the top of page 73 in Benedetto for backward and forward

metrics are recursive with a latency of $O(\log_2 N)$.

35 U.S.C. 103(a) rejection of claims 18, 53 and 77.

The log-BCJR algorithm taught in Benedetto starting on page 71 is a sliding-window

algorithm implemented by tiling an observation interval into subintervals called windows;

and applying a minimum half-window SISO operation on each subinterval of the

window.

35 U.S.C. 103(a) rejection of claim 54, 55, 57, 60, 78, 79, 81, 84, 91, 92, 95, 96, 99 and

100.

Viterbi teaches demodulating the received encoded signal to produce soft information

(See Figure 1 and 3 in Viterbi); and iteratively processing the soft information with one

or more soft-in/soft-output SISO modules (Figure 4 in Viterbi is a decoder having a

feedback loop for iteratively processing soft information according to the iterative

algorithm of Figure 7 in Viterbi; col. 3, lines 66-67 and col. 4, lines 66-67 in Viterbi teach

clearly suggest the intent to replace to replace the MAP decoders typically used in a

turbo decoder with SOVA decoders; Note: a SOVA decoder is inherently a decoder

accepting soft inputs to perform Viterbi's algorithm to produce soft outputs; hence a

SOVA decoder **is also a SISO decoder**; the Examiner suggests the Hagenauer treatise

included in the Examiner's PTO-892 for teachings on SOVA decoders), at least one

SISO module using a tree structure arranged to perform parallel prefix and suffix

operations to compute forward and backward state metrics (the Forward Viterbi

Decoder 24 in Figure 4 of Viterbi teaches a first SISO module using the Trellis tree

structure of Figure 5 to perform parallel prefix operations to compute forward state

metrics $\alpha_k(s)$ in Equation 5 in col. 6 of Viterbi and the Backward Viterbi Decoder 24 in

Figure 4 of Viterbi teaches a second SISO module using the Trellis tree structure of

Figure 5 to perform parallel suffix operations to compute backward state metrics $\beta_{k-1}(s')$

in Equation 6 in col. 6 of Viterbi; Note: the Applicant defines prefix operations

recursively as $z_0=y_0$ and $z_i= y_0\otimes ...\otimes y_i$, it is easy to see that Equation 5 in col. 6 of

Viterbi is a prefix operation by letting $z_0=y_0=\alpha_0$, k=i and $z_i =\alpha_i(s)y_i(s',s)$ when $\otimes$ is

multiplication, likewise equation 6 of Viterbi satisfies suffix operations if the suffix

operations are defined as on page 21 of the Applicant's disclosure).

In addition Viterbi teaches receiving an input signal corresponding to one or more

outputs of a finite state machine (A convolutional encoder is inherently an FSM hence

the received input signal corresponds to one or more outputs of a finite state machine:

Note: a Trellis is also an FSM for the convolutional code).

Viterbi teaches receiving an input signal corresponding to output from one or more block

encoding modules (col. 7, lines 40-44 in Viterbi teach one or more block encoding

modules; Note: turbo encoders and SCIC codes are comprised of one or more block

encoding modules).

However Viterbi does not explicitly teach the specific use of a demodulator adapted to

receive as input a signal encoded by a finite state machine (FSM) and to produce soft

information relating to the received signal.

Benedetto, in an analogous art, teaches the Soft Demodulator of Figure 2 on page 66 of

Benedetto receives an encoded signal and demodulates the received encoded signal to

produce soft information; Note: convolutional or the turbo code taught in the Benedetto

paper is produced using sequential logic, i.e., an FSM.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to modify Viterbi with the teachings of Benedetto by including use

of a demodulator adapted to receive as input a signal encoded by a finite state machine

(FSM) and to produce soft information relating to the received signal. This modification

would have been obvious to one of ordinary skill in the art, at the time the invention was

made, because one of ordinary skill in the art would have recognized that use of a

demodulator adapted to receive as input a signal encoded by a finite state machine

(FSM) and to produce soft information relating to the received signal would have

provided the opportunity to provide required soft information to the soft decoders in the

Viterbi patent (Note: a SOVA decoder is inherently a decoder accepting soft inputs to

perform Viterbi's algorithm to produce soft outputs; hence a SOVA decoder **is also a**

SISO decoder; the Examiner suggest the Hagenauer treatise included in the

Examiner's PTO-892 for teachings on SOVA decoders).

35 U.S.C. 103(a) rejection of claims 56 and 80.

Figure 6 on page 79 of Benedetto teaches using soft output of a first SISO as soft input

to another SISO.

35 U.S.C. 103(a) rejection of claims 58 and 82.

The max-sum operations at the top of page 73 in Benedetto for backward and forward

metrics are recursive with a latency of $O(\log_2 N)$.

35 U.S.C. 102(e) rejection of claims 59 and 83.

Note: a Brent-Kung tree is a specific obvious embodiment of a Trellis tree structure.
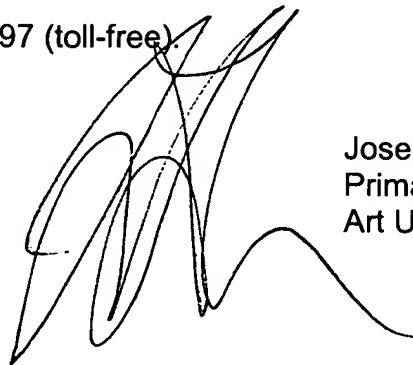
Conclusion

7.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. Hagenauer, J.; Hoeher, P.; A Viterbi algorithm with soft-decision

outputs and its applications; IEEE GLOBECOM, 27-30 Nov. 1989; Page(s): 1680 –

1686; vol.3 (Note: a SOVA decoder is inherently a decoder accepting soft inputs to perform Viterbi's algorithm to produce soft outputs; hence a SOVA decoder **is also a SISO decoder**; the Examiner suggests the Hagenauer treatise included in the Examiner's PTO-892 for teachings on SOVA decoders).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133

JOSEPH TORRES
PRIMARY EXAMINER